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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,800	08/30/2000	Paul S. Neuman	RA 5290(33012/289/101)	1186

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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	5

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,800	NEUMAN, PAUL S.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed March 17, 2003 in response to PTO Office Action mailed December 13, 2002. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, claims 1, 6 and 8 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-20 are now pending in this application.

3. The objection to the specification has been withdrawn due to the amendment filed March 17, 2003.

4. The rejection of claims 1-20 as in the Office action mailed December 13, 2002 (Paper No. 3) is respectfully maintained and reiterated below for Applicant's convenience.

5. The newly added limitation introduced into the independent claims does not affect the scope of the rejection because the recitation "a level three cache memory responsively coupled to said level two cache memory" does not remove the references from reading upon the claims because the system recited in Lynch provides a common memory bus (i.e., system bus) which provides access to and from the main memory through the e-cache (i.e., level two cache) via the common memory bus as detailed in column 1, lines 26-27 and column 3, lines 34-35.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Lynch et al. (US6,061,766).

As per claim 1, Lynch discloses a data processing system having a system bus {*i.e., common memory bus*} and having a processor with a level one cache memory {*i.e., CPU 302, on-board caches 308*} responsively coupled to a level two cache memory {*i.e., cache 306*} which is responsively coupled to a level three cache memory {*i.e., main memory*} [Fig. 3; col. 3, lines 36-43]; and having a circuit for Snooping said system bus [col.3, line 60]; and first logic which invalidates a corresponding level one cache memory location {*i.e., processor invalidate data in their own memories (or on-chip caches)*} in response to either a non-local write or write ownership request {*i.e., request for exclusive use*} [col. 1, lines 40-48, 53-55].

As per claim 2, Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claim 3, Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

As per claim 4, Lynch discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [Fig. 4, steps 408-420].

8. Claims 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US6,397,300).

As per claim 6, Arimilli discloses a data processing system comprising a level one cache memory {*i.e., CPU 150, L1 cache 200*}; a level two cache memory responsively coupled to said level one cache memory {*i.e., L2 cache 202*}; a level three memory responsively coupled to said level two cache memory {*i.e., main memory coupled to L2 cache 202*} [Fig. 4, col. 8, lines 30–49]; and a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write {*i.e., if hit in upper level cache, cache line in upper level cache invalidated*} [col. 5, lines 12-25].

As per claims 11 and 16, Arimilli discloses a method of maintaining validity of data within a level one cache memory of a processor responsively coupled to a level two cache memory which is responsively coupled to a system memory bus [Fig. 4, *L1 cache 200, L2 cache 202, system bus 105*] comprising: formulating a write request {*i.e.,*

issuing store operation} [col. 12, lines 10]; first experiencing a level one cache memory miss in response to said write memory request [col. 12, line 18]; second experiencing a level two cache memory hit in response to said first experiencing step [col. 9, lines 33-34, col. 12, lines 54-56]; and invalidating a portion of said level one cache memory corresponding to said write memory request in response to said second experiencing step {*i.e., L2 cache controls update and invalidation of L1 cache*} [col. 10, line 45 - col. 11, line 19].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al. (US6,061,766) and Hazawa (US4,891,809).

As per claim 5, Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Lynch does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Lynch and Hazawa before him at the time the invention was made, to modify the system of Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

11. Claims 7-9, 12-14 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Lynch et al. (US6,061,766).

As per claims 7, 12 and 17, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership {*i.e., only requests for exclusive use which match cache tags are invalidated*} [Fig. 4; col. 4, lines 19-30].

As per claims 8, 13 and 18, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26].

As per claims 9, 14 and 19, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss.

Lynch discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [Fig. 4, steps 408-420].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Lynch before him at the time the invention was made, to modify the system of Arimilli to include a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership, logic which invalidates said corresponding cache memory location in response to a SNOOP hit, logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss because it would have provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system as taught by Lynch by invalidating a data object a data object contained in the on-chip cache and checking for

the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

12. Claims 10, 15 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Hazawa (US4,891,809).

As per claims 10 and 15, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col. 3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Hazawa before him at the time the invention was made, to modify the system of Arimilli to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

Response to Arguments

13. Applicant's arguments filed March 17, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

(a) Lynch admittedly does not show a common memory bus and neither Lynch nor Arimilli teaches or suggests a level three cache memory.

Examiner respectfully traverses applicant's arguments for the following reasons. Lynch clearly teaches a system wherein a common memory (*i.e., L3 cache*) can only be accessed through an e-cache (*i.e., L2 cache*) and wherein processor(s) share the main memory via the common memory bus (*i.e., system bus*) and the e-cache as detailed in col. 1, lines 26-30 and col. 3, lines 34-38. Thus, in the Lynch reference, if the common memory can only be accessed through the e-cache, these two elements must be coupled to each other. Furthermore, if the processors share the main memory via the common memory bus and the e-cache, the common memory bus must be positioned between the main memory and the e-cache. Consequently, it can be clearly seen that the common memory bus constitutes a system bus as is well known in the art and provides the connection (*or coupling*) between the main memory and the e-cache.

Applicant's assertion that Lynch or Arimilli does not teach or suggest a level three cache memory is clearly erroneous. As is well know in the art, it is customary in a cache hierarchy comprising three levels to use the main memory as the upper level cache or L3 cache. Examiner would like to point applicant's attention to Fig. 1 and 2 of the Fletcher et al (4,442,487) reference submitted as IDS on December 18, 2000 where such a configuration is used. The cache hierarchy is nothing more than a small, high

speed memory unit used to improve the performance of a CPU. The higher the cache level, the slower the access as the memory capacity increases.

(b) Lynch says nothing of "mode 3 requests" and says nothing of "ownership".

Examiner would like to point out that the snoop requests of Lynch indicates the snooping of level three caches since the Lynch reference indicates the presence or absence of the snooped data object in each cache as detailed in column 4, lines 30-32. The assertion that Lynch says nothing of "ownership" is simply erroneous. Examiner would like to point out that in the exclusive state, a variable or cache block exists only in one cache. When a processor is granted exclusive use of a data object, all other processors invalidate that data in their *own* memories. Thus, if the block is present in only one cache, it can clearly be seen that the block is owned by this cache.

(c) In claim 3, Examiner cites the same structure used to show the "second logic".

Considering that logic steps are used as aids in showing the way a proposed program will work and that each step processes information by performing a logical operation on it, it is clearly obvious that any computer system uses a combination of logics to produce outputs based on the rules of logic it is designed to follow. Thus, multiple logics must be used as part of the system to obtain desired results.

(d) Lynch does not teach a step that "retrieves or records data".

Examiner agrees with applicant that the portion cited by Examiner does not teach a step that "retrieves or records data". However, Examiner would like to point out that a snoop request is issued when a processor desires exclusive use of an object from main memory as detailed on page 3, column 56-58. Therefore, the processor must retrieve the object from main memory for its exclusive use as is well known in the art. Further, the system cannot afford to waste resources in performing snoops if it was not for the purpose of retrieving or storing data.

(e) Arimilli does not teach an invalidation requiring "a simultaneous level two cache write".

Examiner respectfully traverses applicant's argument. Examiner would like to point out that Arimilli discloses that the store operation is passed to lower level cache whether it hits or misses in an upper level cache as detailed in column 5, lines 10-16.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "*simultaneous write*") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(f) Arimilli does not teach "experiencing a level two cache memory hit in response to experiencing a level one cache miss in response to a write request".

Examiner respectfully traverses applicant's argument. Examiner would like to point out that Arimilli discloses this feature as detailed in column 5, lines 10-25. As can be seen, Arimilli discloses that the store operation is passed to lower level cache whether it hits or misses in an upper level cache. Misses in L1 cache automatically requires the system to send the request to the L2 cache and so on as is well known in the art.

Claim 16 is directed to the same invention as claim 11 and, as such, does not require a different or separate base of rejection.

(g) In response to applicant's argument that the examiner's conclusion of obviousness is based upon unsupported conclusion, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, the conclusion and motivation is extracted directly from the reference of record. Therefore, the motivation is proper.

Hazawa discloses invalidating levels of cache based on error detection as detailed in column 1, lines 40-50 and column 3, lines 19-48.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
April 8, 2003